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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,331	01/13/2001	Masatoshi Ishikawa	876564/0083	2692

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EXAMINER	
AZARIAN, SEYED H	
ART UNIT	**PAPER NUMBER**
2625	6

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,331	MASATOSHI ISHIKAWA	
	Examiner	Art Unit	
	Seyed Azarian	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-14, are rejected under 35 U.S.C. 103(a) as being unpatentable over Numazaki (U.S. patent 5,900,863) in view of Terada (U.S. patent 5,161,140).

Regarding claim 1, Numazaki discloses an image detection processor comprising; a plurality of image detection processing elements; each said image detection processing element (column 9, line 61 through column 10, line 12, gravity center detecting and image detection);

a photodetector, a converter for converting signals from said photodetector into digital signals (column 36, lines 48-54, A/D converter converts the signals into digital data);

an adder, which receives, said digital signals as an input arranged on a plane (column 28, lines 54-67, refer to adder and column 43, lines 52-64, pixel values which the output currents of the photodetector arry).

However Numazaki is silent about "cumulative adder". On the other hand Terada teaches the first adder counter cumulatively adds the 4-bit difference data with polarity bit to form an 8-bit current track position data (column 6, lines 6-21).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify detecting object in Numazaki invention according to the teaching of Terada because it provides logic circuit used in a computer to add binary digits and produces two outputs, which can easily be implemented in an image detection processing to achieve a better speed and hence a better image quality.

Regarding claim 2, Numazaki discloses an image detection processor comprising; a plurality of image detection processing elements; each said image detection processing element photodetector, converter for converting signals from said photodetector into digital signals, and a first adder which receives said digital signals as an input arranged in a matrix form on a plane, first cumulative adders formed by connecting said first adders of a plurality of said image detection processing elements in respective rows in sequence (see claim 1, also column 20, lines 19-32, LEDs arranged in rows and columns, forming a LED matrix).

However Numazaki is silent about "second cumulative adder". On the other hand Terada teaches circuit transmits the 6-bit difference data indicating the speed data to second adder-counter along with polarity data (column 6, line 57 through column 7, line 6).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify detecting object in Numazaki invention according to the teaching of Terada because it provides logic circuit used in a computer to add binary digits and produces two outputs, which can easily be implemented in an image detection processing to achieve a better speed and hence a resultant better image quality.

Regarding claim 4, Numazaki discloses a n image detection processor, wherein several digital signals selected from said digital signals of said image detection processing elements are inputted to said first cumulative adders by said control circuit and said processed data outputted from said second cumulative adder is set to a partial sum for obtaining an N-order moment of focused images focused to a group of said image detection processing elements, where N is an integer of at least one (column 22, lines 1-21, the numbers and time interval).

Regarding claim 6, Numazaki discloses an image detection processor, wherein said digital signals outputted from a specific image detection processing element is generated based on an output from said photodetector of said photodetector of said specific image detection processing element and said digital signals from a plurality of image detection processing elements (column 19, line 61 through column 20, line 6, generating an output with specific waveform (or specific image)).

Regarding claim 7, Numazaki discloses an image detection processor, wherein all elements are formed into one chip (column 26, lines 27-34, LED chips).

Regarding claims 3, 5,11 and 13, it recites similar limitation as claim 2, are similarly analyzed.

Regarding claims 8, 12 and 14, it recites similar limitation as claims 4, 6 and 7, are similarly analyzed.

Regarding claims 9 and 10, it recites similar limitation as claim 1, are similarly analyzed.

Other prior art cited

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. patent (5,852,491) to Freifeld is cited for Distance measuring apparatus.

U.S. patent (4,240,727) to Lermann et al is cited for focusing system.

U.S. patent (5,150,957) to Walker et al is cited for real time registration weave correction system.

U.S. patent (5,347,590) to Nonnweiler et al is cited for spatial filter for an image processing system.

U.S. patent (5,450,146) to Chedeville et al is cited for high fidelity reproduction device for cinema sound.

U.S. patent (4,186,301) to Basire et al is cited for automatic focus control for a microscope.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seyed Azarian whose telephone number is (703) 306-5907. The examiner can normally be reached on Monday through Thursday from 6:00 a.m. to 7:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta, can be reached at (703) 308-5246. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR.
Status information about the PAIR system, see http:// pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jayanti K. Patel
Primary Examiner

Seyed Azarian
Patent Examiner
Group Art Unit 2625
February 9, 2004